6. DESIGN OF ACTIVE FILTERS (LPF, HPF)

**Aim:** To design and test the low pass filter and high pass filter using op-amp

**Apparatus:**

1) Op-Amp (μA 741) - 2 No’s
2) DC Power Supply (12-0-12) V
3) CRO (0-20MHz range)
4) Signal Generator (0 to 1MHz range)
5) Bread board
6) Resistors and capacitors

**Theory:**

(a) Low pass filter:

![Pass Band Diagram](image)

(a) frequency response

![Low Pass Filter Circuit](image)

(b) Low pass filter using op-amp
The frequency response of a low-pass filter is shown in Fig. 1. The filter has a constant gain from 0 Hz to a high cut-off frequency $f_H$. At $f_H$ the gain is down by 3 dB; after $f > f_H$ the gain decreases with an increase in input frequency at a rate of $-20$ dB per decade. The frequencies between 0 Hz and $f_H$ are known as pass band frequencies, whereas the range of frequencies those beyond $f_H$ are called stop band frequencies.

**Design Procedure:**

1. Select high cut-off frequency $f_H$ of the filter. Let $f_H = 700$ Hz.
2. Select value of C less than 1 $\mu$F. (As the maximum value of ceramic capacitor available is 1 $\mu$F). Let $C = 0.01$ $\mu$F.
3. Calculate $R$ from Eq. (1),
   \[ f_H = \frac{1}{2\pi RC} \]  
   \[ (1) \]
   
   For $f_H = 700$ Hz and $C = 0.01$ $\mu$F, from Eq. (1) $R = 22.7$ k$\Omega$.
   Select nearest value of standard resistance available $R = 22$ k$\Omega$.
4. Select $R_1$ and $R_2$ such that required pass band gain is obtained.
   Pass band gain = $1 + (R_2/R_1)$.
   Let $R_2 = R_1 = 10$ k$\Omega$ for a pass band gain of 2.
5. Final values of components:
   \[ R_1 = 10 \text{ k}\Omega, \quad R_2 = 10 \text{ k}\Omega, \quad R = 22 \text{ k}\Omega, \quad C = 0.01 \mu\text{F}, \quad f_H = 700 \text{ Hz}. \]

**Lowpass filter experimental procedure:**

1) Vary the input frequency at regular intervals and note down the output response from the CRO.
2) Calculate the gain in dB.
3) Verify practical and theoretical cutoff frequency
4) Plot the frequency response on semi-log sheet.
Second order Low pass filter

Where

\[ A_F = 1 + \frac{R_p}{R_1} = \text{Passband gain of the filter} \]
\[ f = \text{frequency of the input signal} \]
\[ f_H = \frac{1}{2\pi\sqrt{R_2^2R_3C_1C_2}} = \text{high cutoff frequency (Hz)} \]

b). High pass filter:

![Diagram of a high pass filter](image)

**Fig. 1 Frequency Response**

**Fig. 2 Circuit Diagram**
The frequency response of a high-pass filter is shown in Fig.1. The filter has a constant gain above the low cut-off frequency $f_l$. At $f_l$ the gain is down by 3 dB the passband gain; below $f < f_l$ it decreases with an increase in input frequency at a rate of $-20$ dB per decade. The frequencies above $f_l$ are known as passband frequencies; whereas as the frequencies from 0 Hz to $f_l$ are called stopband frequencies.

**Design Procedure:**

1. Select low cut-off frequency $f_l$ of the filter. Let $f_l = 800$ Hz.
2. Select value of $C$ less than 1 $\mu$F. (As the maximum value of ceramic capacitor available is 1 $\mu$F). Let $C = 0.01$ $\mu$F.

3. Calculate $R$ from Eq. (1).
   \[ f_l = \frac{1}{2\pi RC} \]  
   (1)
   For $f_l = 700$ Hz and $C = 0.01$ $\mu$F, from Eq. (1) $R = 22.7$ k$\Omega$.
   Select nearest value of standard resistance available $R = 22$ k$\Omega$.
4. Select $R_3$ and $R_F$ such that required pass band gain is obtained.
   Pass band gain = $1+(R_F/R_3)$.
   Let $R_3 = R_F = 10$ k$\Omega$ for a pass band gain of 2.
5. Final values of components:
   $R_3 = 10$ k$\Omega$, $R_F = 10$ k$\Omega$, $R = 22$ k$\Omega$, $C = 0.01$ $\mu$F, $f_l = 700$ Hz.

**Highpass filter experimental procedure:**

1) Vary the input frequency at regular intervals and note down the output response from the CRO.
2) Calculate the gain in dB.
3) Verify practical and theoretical cutoff frequency
4) Plot the frequency response on semi-log sheet
Second order high pass filter

The voltage gain magnitude of the second order high pass filter is

\[ \frac{V_o}{V_{in}} = \frac{A_f}{\sqrt{1 + \left(\frac{f_l}{f}\right)^4}} \]

**Result:**

**Practical values**
Cut-off Frequency of low pass filter =
Cut-off Frequency of high pass filter =

**Theoretical values:**
Cut-off Frequency of low pass filter =
Cut-off Frequency of high pass filter =

**Review Questions:**

1. What happens when the no. of stages of filter increases?
2. What is the necessity of Op-Amp in designing of Active filters
3. What is the another name for butter worth low pass /high pass filter
4. Mention the application of Butterworth filter
5. What is the difference between First-order filter and second order filter?

Signature of Instructor
7. STUDY OF OP-AMP COMPARATOR

Aim: To study the comparator operation using Op-Amp.

Apparatus:
1. Op-Amp (µA -741) - 2 No’s.
2. DC Power Supply (12 -0 - 12) V
3. Bread board.
4. Resistors (4.2k, 6.3k)- 2 No’s.
5. LED’s.

Procedure:
1. Connect the circuit as shown in the figure.
2. Apply voltages according to table given and verify the LED’s.

### If Vcc = 6V:

<table>
<thead>
<tr>
<th>Input(Volts)</th>
<th>LED3</th>
<th>LED2</th>
<th>LED1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Less than 2V</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>Less than 4V &amp; More than 2V</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>More than 4V</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>
Comparison between Schmitt trigger and comparator

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Schmitt Trigger</th>
<th>Comparator</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>The feedback is used.</td>
<td>No feedback is used.</td>
</tr>
<tr>
<td>2.</td>
<td>Op-amp is used in closed loop mode.</td>
<td>Used in open loop mode.</td>
</tr>
<tr>
<td>3.</td>
<td>No false triggering.</td>
<td>False Triggering.</td>
</tr>
<tr>
<td>4.</td>
<td>Two different threshold voltages exists as ( V_{UT} &amp; V_{LT} )</td>
<td>Single reference voltage ( V_{ref} ) or ( -V_{ref} ).</td>
</tr>
<tr>
<td>5.</td>
<td>Hysteresis exists.</td>
<td>No Hysteresis exists.</td>
</tr>
</tbody>
</table>

**Result:**

**Review Questions:**

1) What is the principle of comparator?
2) Which type of circuit use comparator?
8. APPLICATIONS OF 555 TIMER

**Aim:** To study the applications of 555 timer.

**Apparatus:**
1. IC 555
2. power supply
3. CRO
4. Resistors
5. capacitors
6. connecting wires
7. bread board

**Theory**
(a) **Pin Diagram of 555:**

![555 Timer IC Diagram](image)

(b) **Pin descriptions for the 555:**

<table>
<thead>
<tr>
<th>Pin No</th>
<th>Description</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ground</td>
<td>DC Ground</td>
</tr>
<tr>
<td>2</td>
<td>Trigger</td>
<td>The trigger pin triggers the beginning of the timing sequence. When it goes LOW, it causes the output pin to go HIGH. The trigger is activated when the voltage falls below 1/3 of +V on pin 8.</td>
</tr>
<tr>
<td>3</td>
<td>Output</td>
<td>The output pin is used to drive external circuitry. It has a &quot;totem pole&quot; configuration, which means that it can source or sink current. The HIGH output is usually about 1.7 volts lower than +V when sourcing current. The output pin can sink up to 200mA of current. The output pin is driven HIGH when the trigger pin is taken LOW. The output pin is driven LOW when the threshold pin is taken HIGH, or the reset pin is taken LOW.</td>
</tr>
<tr>
<td>4</td>
<td>Reset</td>
<td>The reset pin is used to drive the output LOW, regardless of the state of the circuit. When not used, the reset pin should be tied to +V.</td>
</tr>
<tr>
<td>5</td>
<td>Control Voltage</td>
<td>The control voltage pin allows the input of external voltages to affect the timing of the 555 chip. When not used, it should be bypassed to ground through an 0.01uF capacitor.</td>
</tr>
</tbody>
</table>
Threshold
The threshold pin causes the output to be driven LOW when its voltage rises above 2/3 of +V.

Discharge
The discharge pin shorts to ground when the output pin goes HIGH. This is normally used to discharge the timing capacitor during oscillation.

+V
DC Power - Apply +3 to +18VDC here.

(C)Block Diagram of 555 Timer:

(d). Applications of 555 Timer:
1. Astable Multivibrator

This circuit diagram shows how a 555 timer IC is configured to function as an astable multivibrator. An Astable multivibrator is a timing circuit whose 'low' and 'high' states are both unstable. As such, the output of an astable multivibrator toggles between 'low' and 'high' continuously, in effect generating a train of pulses. This circuit is therefore also known as a 'pulse generator' circuit.
In this circuit, capacitor $C_1$ charges through $R_1$ and $R_2$, eventually building up enough voltage to trigger an internal comparator to toggle the output flip-flop. Once toggled, the flip-flop discharges $C_1$ through $R_2$ into pin 7, which is the discharge pin. When $C_1$’s voltage becomes low enough, another internal comparator is triggered to toggle the output flip-flop. This once again allows $C_1$ to charge up through $R_1$ and $R_2$ and the cycle starts all over again.

$C_1$’s charge-up time $t_1$ is given by: $t_1 = 0.693(R_1+R_2) C_1$. $C_1$’s discharge time $t_2$ is given by: $t_2 = 0.693(R_2) C_1$. Thus, the total period of one cycle is $t_1+t_2 = 0.693 C_1 (R_1+2R_2)$.

The frequency $f$ of the output wave is the reciprocal of this period, and is therefore given by: $f = 1.44/(C_1 (R_1+2R_2))$, wherein $f$ is in Hz if $R_1$ and $R_2$ are in megaohms and $C_1$ is in microfarads.

2. Monostable Multivibrator

![Monostable Multivibrator Diagram]

This circuit diagram shows how a 555 timer IC is configured to function as a basic monostable multivibrator. A monostable multivibrator is a timing circuit that changes state once triggered, but returns to its original state after a certain time delay. It got its name from the fact that only one of its output states is stable. It is also known as a 'one-shot'. In this circuit, a negative pulse applied at pin 2 triggers an internal flip-flop that turns off pin 7's discharge transistor, allowing $C_1$ to charge up through $R_1$. At the same time, the flip-flop brings the output (pin 3) level to 'high'. When capacitor $C_1$ as charged up to about 2/3 Vcc, the flip-flop is triggered once again, this time making the pin 3 output 'low' and turning on pin 7’s discharge transistor, which discharges $C_1$ to ground. This circuit, in effect, produces a pulse at pin 3 whose width $t$ is just the product of $R_1$ and $C_1$, i.e., $t=R_1C_1$.

The reset pin, which may be used to reset the timing cycle by pulling it momentarily low, should be tied to the Vcc if it will not be used.

**Result:**

**Review questions:**

1. What is the basic principle of 555 to act like a astable multivibrator?
2. How astable mode of 555 can be changed to square wave generator?
3. How the duty cycle of astable multivibrator using IC555 can be changed?
4. What is the basic principle of 555 to act like a monostable multivibrator?
5. What is the difference between astable multivibrator and mono stable multivibrator using IC 555